REMARKS

The above-identified patent application has been amended and Applicants respectfully request the Examiner to reconsider and again examine the claims as amended.

Claims 1, 2 and 4-41 are pending in the application. No claims are yet allowed. Claims 1, 2 and 4-41 are rejected. Claims 1 and 4 are amended herein. Claim 9 has been cancelled and no new claims have been added by this amendment.

Applicant notes that the Examiner has objected to the drawings. The Examiner has taken the position that the third semiconductor structure recited in claim 41 must be shown in the drawings or cancelled from the claim. The second sentence of 35 U.S.C. 113 addresses the situation wherein a drawing is not necessary for the understanding of the invention, but the subject matter sought to be patented admits of illustration and no drawing was submitted on. In this case, it is Applicant's position that the subject matter sought to be patented with claim 41 does not admit of illustration. It is Applicants position that in view of drawing Figs. 1-4 which all illustrate an interface disposed to accept a third semiconductor structure as well as at least the text which accompanies Fig. 2, that no drawing change is required.

The Examiner objected to Claim 4 as depending from a cancelled claim (i.e. claim 3). Applicants' have amended claim 4 to depend from claim 1.

The Examiner objected to Claim 9 as containing certain informalities. Applicants' have cancelled claim 9 and thus the claim will not be discussed.

The Examiner rejects Claims 1, 2 and 4-41 under 35 U.S.C. §102(b) as being anticipated by Kato (U.S. Pat. No. 4,939,568).

Applicants submit that claim 1 is patentably distinct over the cited reference since the reference neither describes nor suggests "...a first device layer having first and second opposing surfaces ...including ...a dielectic material ... and a first conductive via ... a conductive interface

having first and second opposing surfaces with the first surface disposed over at least a portion of the first surface of the first substrate such that at least a portion of the conductive interface is coupled to at least a portion of the first end of the first conductive via ... a second device layer including ... a second substrate... an insulating material having a first surface disposed against a second surface of the conductive interface and a second opposing surface disposed against a first one of the first and second opposing surfaces of the substrate... a second conductive via provided in the second device layer, said second conductive via having a first end directly coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions as called for in Claim 1.

To sustain a rejection under 35 U.S.C. §102, a single reference must disclose each and every element of the claimed invention. In this case, the Kato reference fails to describe a structure in which two semiconductor structures are coupled through a conductive interface with each of the semiconductor structures containing conductive vias which electrically couple the respective semiconductor structures to the conductive interface.

In particular, the Kato reference does not describe a second device layer which includes a substrate and an insulating material having a first surface disposed against a second opposing surface of the conductive interface and a second opposing surface disposed against a ... surface[s] of the substrate.

The Examiner equates interconnect terminal 7b to the conductive interface recited in Applicants' claim 1 and the Examiner equates insulating layers 41, 45 of Kato to the insulating layer recited in Applicants' claim 1. The Kato interconnect terminal 7b has one end coupled to conductive via 6a and an opposite end coupled to wiring layer 42. Thus, insulating layers 41, 45 of Kato do not have "a first surface disposed against a second opposing surface of the conductive interface" as called for in Claim 1.

Also claim 1 calls for "...a second conductive via provided in the second device layer, said second conductive via having a first end directly coupled to the conductive interface...." The

Examiner equates conducting post 4a of Kato to the second conductive via recited in Applicants' claim 1. However, conducting post 4a is not directly coupled to the conductive interface. Thus, this claim limitation is not met.

In view of the above, Applicants submit that Claim 1 is patentably distinct over the Kato reference.

Claims 2, 4-8 and 10-16 each depend either directly or indirectly from base claim 1 and thus these claims are patentably distinct over the cited reference generally for the reasons discussed above in conjunction with claim 1.

Applicants submit that Claim 17 is patentably distinct over the cited reference since the reference neither describes nor suggests a ... multi-layer integrated semiconductor structure comprising ... at least a first device layer having first and second opposing surfaces... at least a second device layer having first and second opposing surfaces ... a first interface disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layer ... as called for in Claim 17.

Kato neither describes nor suggests a structure in which an interface is disposed between a first surface of a first device layer and a first surface of a second device layer.

The portions of the Kato structure which the Examiner equates to the interface recited in claim 17 are part of the devices. Thus, those portions of the Kato structure which the Examiner equates to the interface recited in claim cannot be disposed between surfaces of the two devices as called for in claim 17.

Claims 18-39 each depend either directly or indirectly from base claim 17 and thus these claims are also patentably distinct over the cited reference generally for the reasons discussed above in conjunction with claim 17.

Applicants submit that Claim 40 is patentably distinct over the cited reference since the reference neither describes nor suggests a ... multi-layer semiconductor structure... comprising ...a first semiconductor wafer ...a second semiconductor wafer ... and at least a first conductive bonding interface segment disposed between the first and second semiconductor wafers...as called for in claim 40.

The Examiner equates the interconnect terminal 7b described in Kato to the conductive bonding interface recited in Applicants' claim 40. Applicants have carefully reviewed the Kato reference and in particular the description of Fig. 3 in Kato, and it is Applicants' position that nothing in the Kato reference suggests that the Kato interconnect terminal 7b could function as a conductive boding interface as called for in Claim 40. It is thus Applicants position that claim 40 is patentably distinct over the cited reference.

If the Examiner maintains his position with respect to claim 40, Applicants respectfully request the Examiner to identify the portions of Kato relied upon for the rejection.

Applicants submit that Claim 41 is patentably distinct over the cited reference since the reference neither describes nor suggests a ...multi-layer semiconductor structure... comprising ...at least a first semiconductor structure ...at least a second semiconductor structure ...a first plurality of conductive bonding interface segments disposed between the first and second semiconductor structures ... at least a third semiconductor structure ...and a second plurality of conductive bonding interface segments disposed between the second and third semiconductor structures ...as called for in claim 41.

The Examiner equates the interconnect terminal 7 described in Kato to the conductive bonding interface recited in Applicants' claim 41. Applicants have carefully reviewed the Kato reference and in particular the description of Fig. 3 in Kato, and it is Applicants' position that nothing in the Kato reference suggests that the Kato interconnect terminal 7 could function as a

conductive boding interface as called for in Claim 41. It is thus Applicants position that claim 41 is patentably distinct over the cited reference.

If the Examiner maintains his position with respect to claim 41, Applicants respectfully request the Examiner to identify the portions of Kato relied upon for the rejection.

The Examiner rejects Claims 1, 2 and 4-8, 12, 13 and 17 under 35 U.S.C. §102(e) as being anticipated by Tiwari (U.S. Pat. No. 6,600,173).

Applicants submit that claim 1 is patentably distinct over the cited reference since the reference neither describes nor suggests a... multi-layer integrated semiconductor structure, comprising ... (a) a first device ...including ... a first substrate ... having a ...plurality of doped regions...a dielectric material having first and second opposing surfaces with the first dielectric material surface disposed over the second surface of the first substrate ... and a first conductive via provided in the dielectric material, the first conductive via having a first end coupled to at least one of the ... plurality of doped regions ... and a second end exposed through the second one of the first and second surfaces of the dielectric material ...(b) a conductive interface ...disposed over at least a portion of the second surface of the dielectric material such that at least a portion of the conductive interface is coupled to at least a portion of the first end of the first conductive via in the first device layer ... (c) a second device layer having first and second opposing surfaces ... with the first surface of the second device layer disposed over the second surface of the conductive interface ...wherein the second device layer is secured to the first device layer via the conductive interface...as called for in claim 1.

The Examiner equates the horizontal portion of conductor 34 to the conductive interface recited in Applicants' claim 1. Claim 1 requires that "...the second device layer is secured to the first device layer via the conductive interface...." It is clear from Tiwari that the horizontal portion of conductor 34 does not secure wafer 20 to wafer 40. Rather, Tiwari at column 2 line 64 through column 3 line 31 explains the bonding process. Please note that at column 3 lines 43 - 47

Tiwari points out that the bonding process described in conjunction with Figs.1-6 is used to form the structures of Figures 7 and 8 in Tiwari.

Also, claim 1 calls for the first conductive via provided in the dielectric material to have a first end coupled to one of the doped regions in the first substrate and a second end exposed through the second one of the first and second surfaces of the dielectric material.

The Examiner equates the Tiwari passivation layer 30 to the dielectric material and the via 32 to the first conductive via recited in Applicants' claim 1. Applicants submit that via 32 does not have an end which is exposed through the second one of the first and second surfaces of the dielectric material as called for in Applicants' claim 1.

In view of the above, Applicants submit that Claim 1 is patentably distinct over the Tiwari reference.

Claims 2, 4-8, 12 and 13 each depend either directly or indirectly from base claim 1 and thus these claims are patentably distinct over the Tiwari reference generally for the reasons discussed above in conjunction with claim 1.

Applicants submit that Claim 17 is patentably distinct over the cited reference since the reference neither describes nor suggests a ... multi-layer integrated semiconductor structure comprising ... at least a first device layer having first and second opposing surfaces... at least a second device layer having first and second opposing surfaces ... a first interface disposed between a first one of the first and second opposing surfaces of the first device layer and a first one of the first and second opposing surfaces of the second device layer ... as called for in Claim 17.

Tiwari neither describes nor suggests a structure in which an interface is disposed between a first surface of a first device layer and a first surface of a second device layer.

The portions of the Tiwari structure which the Examiner equates to the interface recited in claim 17 are part of the wafers themselves. Thus, those portions of the Tiwari structure which the Examiner equates to the interface recited in claim cannot be disposed between surfaces of the two devices as called for in claim 17.

The Examiner rejects Claims 7 - 11 and 14 - 16 under 35 U.S.C. §103(a) as being unpatentable over Kato (U.S. Pat. No. 4,939,568) in view of Nulman (U.S. Pat. No. 5,904,562).

The Examiner asserts that "Kato shows most aspects of the instant invention except for the use of copper to make the first conductive interface." The Examiner relies upon Nulman as teaching that copper is a suitable material to make metallization films and concludes that it would have been an obvious matter of design choice o one having ordinary skill in the art to make the first conductive interface disclosed by Kato of copper as taught by Nulman.

Applicants do not agree that Kato shows most aspects of claim 7 except for the use of copper to make the first conductive interface.

Claim 7 depends from 1 and thus includes each of the limitations of claim 1. Thus, claim 7 calls for ... a second device layer which includes a substrate and an insulating material having a first surface disposed against a second opposing surface of the conductive interface and a second opposing surface disposed against a ... surface[s] of the substrate and an insulating layer having a first surface disposed against a second opposing surface of the conductive interface ...and ... a second conductive via provided in the second device layer [and] having a first end directly coupled to the conductive interface....

Nulman neither describes nor suggests the above features. Thus, the combination of Nulman and Kato cannot render obvious claim 7 since all of the claim limitations are neither described nor suggested in the combination proposed by the Examiner.

To establish a prima facie case of obviousness "...the prior art reference (or prior art references when combined) must teach or suggest all the claim limitations..." (see MPEP §2142). Applicants respectfully submit that in this case, the Examiner has not met this burden in order to establish prima facie obviousness.

Claims 8 , 10, 11 and 14-16 each depend, either directly or indirectly from claim 1 and thus include the limitations of Claim 1. Thus, Applicants submit that Claims 8, 10, 11 and 14-16 are also patentably distinct over the cited references at least for the reasons discussed above in conjunction with Claim 7.

In view of the above Amendments and Remarks, Applicants submit that Claims 1, 2, 4-8, 10-41 and the entire case are in condition for allowance and should be sent to issue and such action is respectfully requested.

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Response or this application.

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Respectfully submitted,

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